YAMAR Electronics Ltd
Preliminary *Data Sheet*

SIG60 - UART over Powerline, for AC/DC-BUS Network

This information is preliminary and may be changed without notice

1 GENERAL

The SIG60 is a second generation transceiver for digital communication over battery powerline. It allows the powerline to be employed for both power and communication, thus eliminating the need for special wires for carrying control and data. The SIG60 uses a unique multiplex digital signaling technology that overcomes the powerline noisy environment. A small footprint integrates most of the external components needed for its operation. A sleep mode puts the device in a power saving mode while it is still capable of sensing the bus for remote wakeup messages from other devices.

The communication over powerline reduces harness and connector size, increases reliability, saves node costs and increases the network throughput.

The powerline new physical layer is useful for a wide range of Automotive, Avionics and Industrial applications. These include sensor readings, actuator activation, doors, seats, mirrors, climate control, lights, Truck-Trailer, etc. The SIG60 contains a UART host interface, modem, line driver and ceramic filter interface.

The SIG60 operates as an AC/DC Powerline transceiver that replaces the RS232 or LIN transceivers thus eliminating the Data wire. Providing up to 115.2 Kbps data rate, the SIG60 offers a significantly improved data rate as compared to the LIN network. The SIG60 network consists of a Master and Salves. Each SIG60 device operates also as a Slave in a multiplex network. Multiple networks may operate concurrently over the same wire by using different carrier frequencies. The SIG60 activates SIG61 smart powerline slave devices

The SIG60 contains a host UART interface, modem, line driver and interface with two external ceramic filters (one of them is optional). The device features a unique Signaling technology to overcome the hostile communication conditions of a vehicle battery line. Sleep mechanism reduces significantly the power consumption when in Sleep mode, while sensing periodically the powerline for wakeup messages from other devices.

Applications

- **Vehicle sub-bus**
- **Batteries / Green Energy cells management network**
- **Sensors Actuators bus**
- **Robotics control network**
- **Steering wheel bus**
- **Mobile Computing**
- **Security Monitoring**
- **Truck-Trailer sub-bus**
- **Door module**
- **Climate control network**
- **Front and back Lights**

Features

- **Noise robust UART / LIN over battery-powerline transceiver.**
- **Six selectable carrier frequencies.**
- **Selectable bit rate between 9.6 Kbps to 115.2 Kbps.**
- **Operates as Master or Slave in a multiplex network.**
- **Multiple networks may operate over the same powerline.**
- **Communicates over wide range of AC/DC voltage lines.**
- **Small size 28 pin QFN package**
- **Sleep Mode for low power consumption.**
- **Eliminates data wire and transceiver in LIN bus.**

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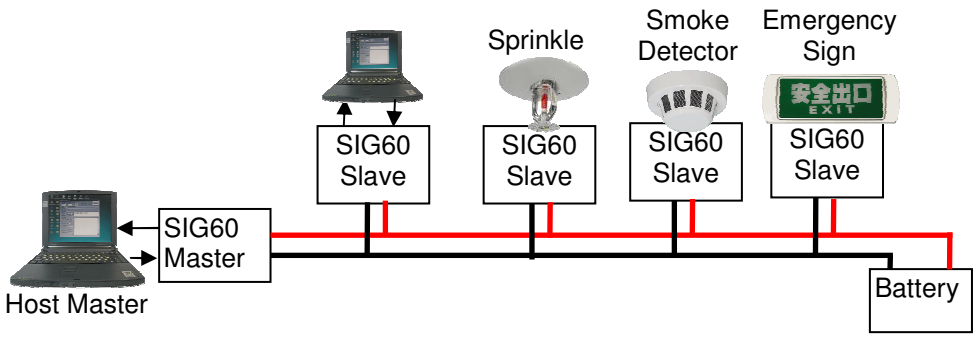

Figure 1.1 - Example of SIG60 in fire protection network

2 OVERVIEW

2.1 Signaling System

The SIG60 device is based on a unique Signaling technology. The device transmits and receives a special signaling carrier, which can be differentiated from the Power line noise. The receiver receives the signaling patterns at a selected frequency and extracts the data from the noisy channel into the original bits. Multiple devices can be used as a network on any of the available carrier frequencies. Multiple channels can operate over the same Powerline noisy lines for additional independent networks.

2.2 Channels and Network

The SIG60-SIG61 network can be set into 16 groups of frequency pairs. When set to such a pair, its two preset frequencies can be easily switched.
Each channel can broadcast asynchronous data messages to other devices on the Power line. The device allows the use of the LIN protocol. The SIG60 device is controlled by a host microprocessor through its UART port.

Channel frequencies:	1.75MHz, 4.5 MHz, 5.5 MHz, 6 MHz, 6.5 MHz, 10.5 MHz and 13MHz.
Data transfer rate:	9.6Kbps to 115.2Kbps.
Cable length:	See 3.3.11.

2.3 The SIG60 Device

The SIG60 device is responsible for transferring messages to all devices over the line. The device handles the communication physical layer and Interference detection. The device communicates with its host via an asynchronous serial port for data transfer and device control. Figure 2.1 outlines the building blocks of the SIG60 device.

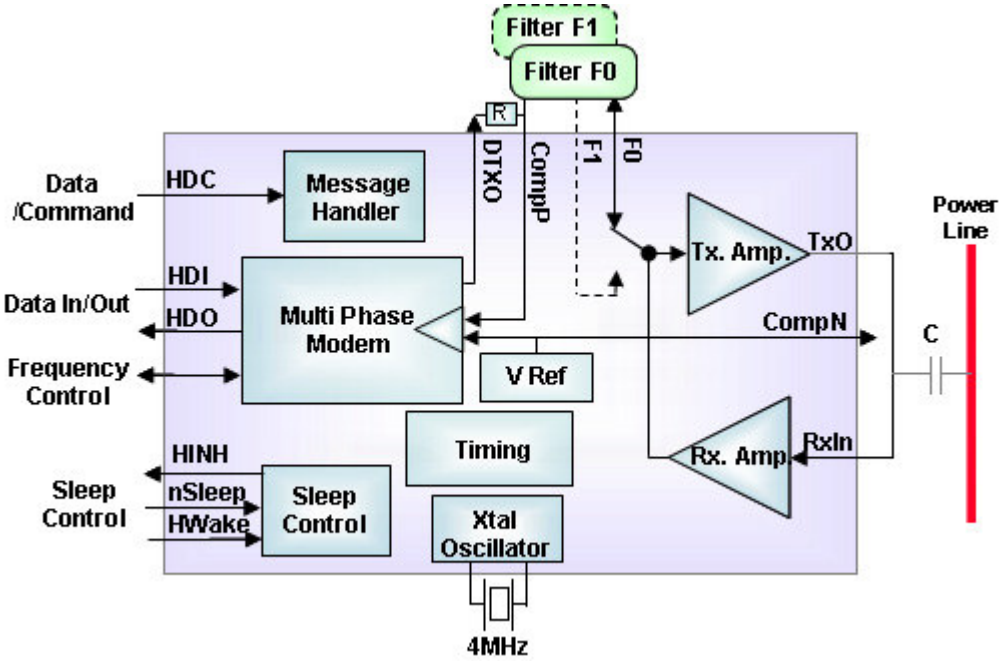

Figure 2.1 - SIG60 logical blocks

2.4 Protocol

The SIG60 may be used in a Master-Slaves network using UART based protocols such as the LIN protocol. The device receives any asynchronous byte (one start and one stop bit), as so, it is transparent to the host while providing additional services for the link and application layers with a built-in Interference detector and frequency management.

2.5 Power Management

Sleep Mode, controlled by the host, saves power by disabling most of the SIG60 internal circuits.
During Sleep Mode, the device is switched ON every 32mSec, for a short period to detect wakeup messages from other devices on the bus. If no activity is detected, the device is switched back to Sleep.

3 SIG60 SIGNALS

The SIG60 Signals are divided into three main functions:

- Host input / output
- Line interface
- Sleep mechanism

Figure 3.1 describes the interconnections between SIG60 its host, the ceramic filters and Power line.

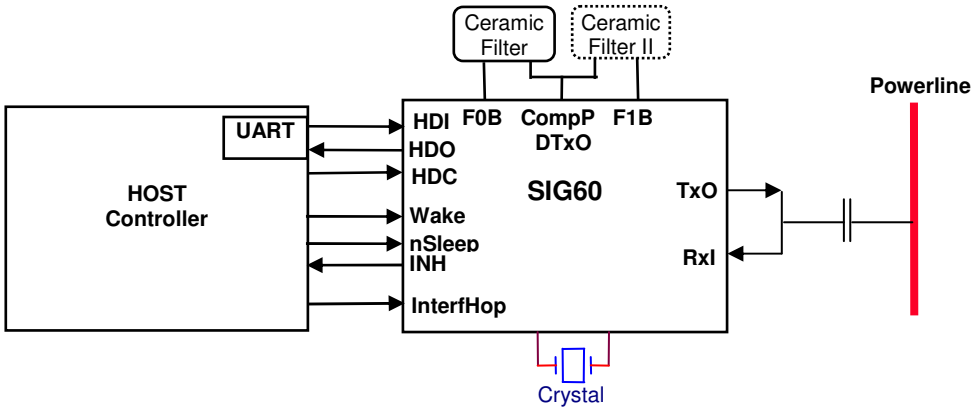

Figure 3.1 - Interfacing the SIG60

Device signals are described in table 3.1.

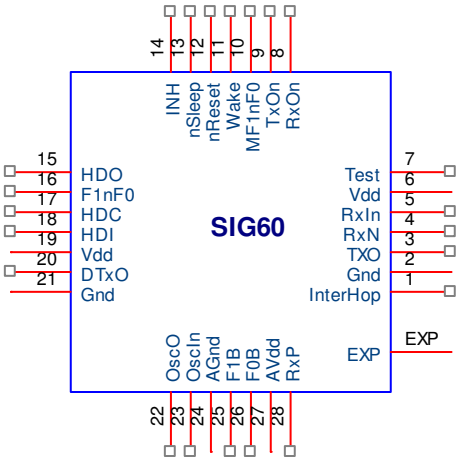

Table 3.1 - Device signals

Pin name	Pin #	Pin type	Description
HDO	15	Output 8mA	Digital data output signal. Output the received data from the powerline to the host.
INH	14	Output 8mA	Inhibit output for enabling the host or an external voltage regulator powering the host. This signal is HIGH in normal and standby mode and LOW in sleep mode.
HDI	18	Input	Data input. Transfer data from the host to the SIG60. When not in use should be pulled Up.
nSleep	13	Input	Sleep control input. Pulling this signal to LOW puts the SIG61 in sleep mode. Should be pulled to Vdd.
HDC	17	Input	Data/Command mode. When LOW, enables read and write to the SIG60's internal registers. When not in use should be pulled Up.
nReset	12	Input, PU	Reset Input
Wake	11	Input	Local wakeup input. Negative or positive edge triggered. This pin can be

			connected to an external switch in the application. When the pin is triggered the device will wake up and send a wake up message to all the devices on the network. When not in use, this pin should be pulled Up or Down
InterfHop	1	Input, Internal pull down	Allows automatic frequency hoping whenever an interference signal is detected on the DC line. When HIGH, detection of interference switches the operating frequency between F0 and F1. If at the new frequency, no reception occurred for 2 sec, the operating frequency is switched back. For designs with a single channel this pin should be tied to ground.
F1nFo	16	Input	Selects between F0 / F1. HIGH – F1, LOW – F0
MF1nF0	10	Output 12mA	Output signal indicates the selected channel. F1=”High”, F0= “Low
Test	7	Input, PD	Should be connected to Gnd
			Line Interface signals
OscO	22	Analog Output	Crystal Output
OscIn	23	Analog Input	Crystal Input
RxN	4	Analog Output	Input to the internal comparator negative pin. Its value is internally pulled to Vdd/2. Bypass RxN to Ground with a 1nF capacitor.
RxP	28	Analog Input	Positive pin input signal. Should be tied to RxN with a 1K Ohm resistor.
DTxO	20	Tristate/ Output 2 mA	Modulated digital transmit signal output to both ceramic filters.
RxIn	5	Analog Input	Receive input from the DC-BUS to the RX operational amplifier. This input is pulled internally to Vdd/2
TxO	3	Analog Output	Transmit output
TxOn	9	Output 12mA	HIGH when the device is transmitting a message
RxOn	8	Output 12mA	HIGH when the device is in receive mode
F0B	26	Analog, Bi directional	F0 External filter I/O. Its value is internally pulled to Vdd/2.
F1B	25	Analog, Bi directional	F1 External filter I/O. Its value is internally pulled to Vdd/2.
			Power signals
Gnd	2,21	Power	Ground
Vdd	6,19	Power	3.3V power
AGnd	24	Power	Analog Ground
AVdd	27	Power	3.3V Analog Power. Separate from Vdd with a 10 Ohm resistor and bypass to Ground with 1nF and 10nF capacitor.
Exp	Exp		May be connected to GND

PD – Pull down resistor 100K ohm +/-%30
PU – Pull up resistor 100K ohm +/-%30

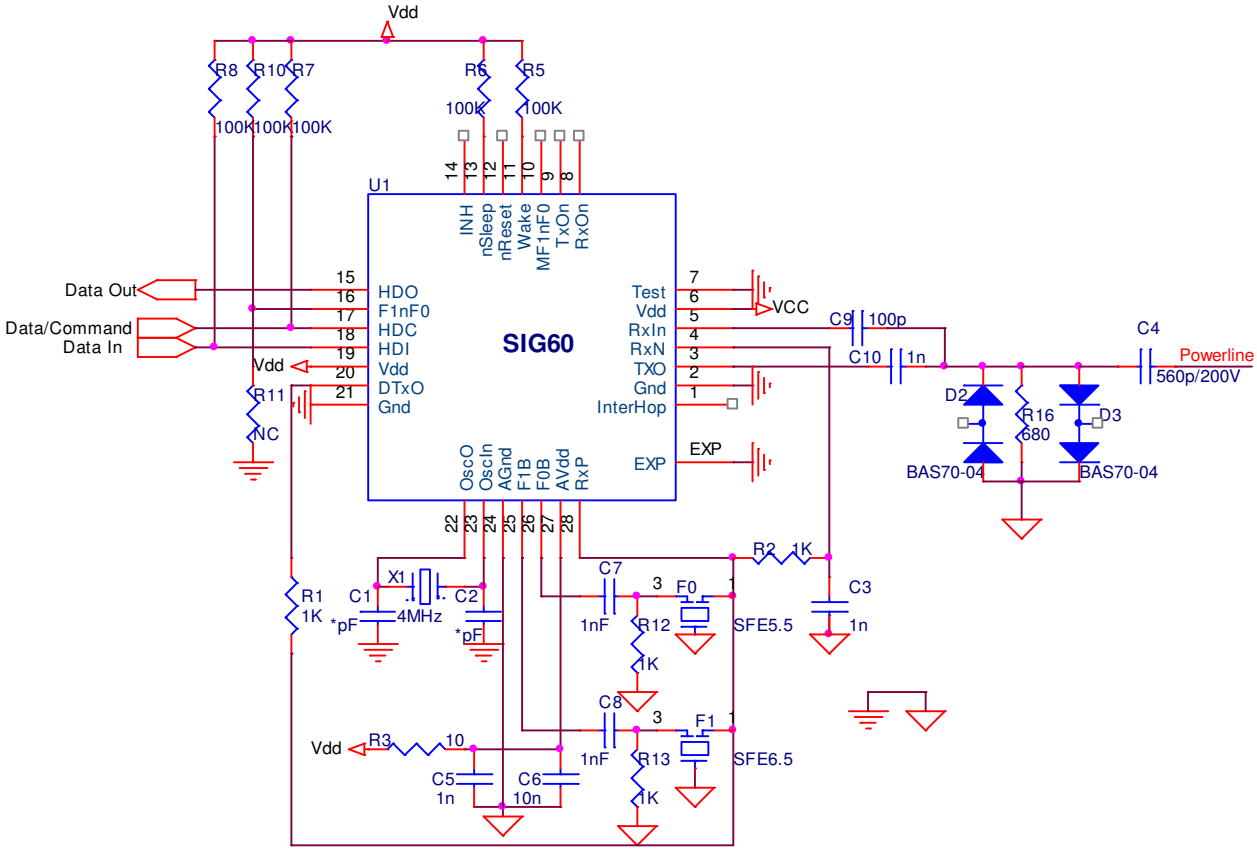

Figure 3.3 – SIG60 schematics example

** C1 and C2 values depend on crystal used. Usually values are between 0pF (NC) to 4.7pF.*

3.1.1 Ceramic Filter Considerations

The SIG60 is designed to operate with one ceramic filter for transmission and reception. However, if switching between two channels is desired, two ceramic filters are required. The minimum allowable bandwidth of the ceramic filters is +/-70 kHz @ 3dB. Narrow bandwidth limits the maximal bit rate.
The SIG60 selectable frequencies meet market available ceramic filters. It is important to select the widest bandwidth available.

Nominal freq.	3 db BW	20db BW	Insertion loss	Stop band attenuation	In/Out imped.	Murata part #	Oscilent part #
MHz	KHz min.	KHz max.	dB max.	dB min.	Ohm		
*1.75						Discrete	
4.50	+/-70	750	6.0	30	1000	SFSL4.5MDB	773-0045
5.50	+/-80	750	6.0	30	600	SFSL5.5MDB	773-0055
6.00	+/-80	750	6.0	30	470	SFSL6.0MDB	773-0060
6.50	+/-80	800	6.0	30	470	SFSL6.5MDB	773-0065
**10.50	+/-150		4.5		330	SFELF10M5JAA001-B0 Discrete filter for 115.2Kbps	
**13.00	280 +/-50		4.5		330	SFELK13M0JA00-B0	

**** 1.75MZ can operate only at 9.6Kbps***

***** 10.5MHz and 13.00MHz operates at 115.2Kbps instead of 9.6Kbps.***

3.1.2 Communication performance

The maximal cable length between extreme devices depends mainly on the AC impedance of loads connected to that line and number of nodes. The power cable length has less effect on communication. The SIG60 needs at least 20mVpp for proper reception. Good communication should be achieved if the transmitted signal can be seen on an oscilloscope at the receiving side within the line noise.

3.2 Frequency Control

The device is designed for operation in two selectable carrier frequencies.
Presence of an interference signal can be read from the device internal register.

3.2.1 Operating Frequency

Either Bit 0 in control register 0 or input pin F1nF0, determines the operating frequency F1 or F0. The current operating frequency can be determined by the status of output pin MF1nF0.

3.2.2 Interference Hoping

When InterfHop pin is high, the device switches its channel automatically whenever an interference signal is detected in the operating frequency. If the device does not receive any data in the new channel it will return to the previous channel after 2Sec. If, again, no data has been received for 2Sec. and the interference has stopped, it will switch frequency once more and will stay at the new channel.

3.3 Crystal Oscillator

The SIG60 is designed to operate with a low cost 4MHz crystal connected between OscIn and OscOut pins.

The values of C5, C6 in Figure 3.3 oscillator circuitry should be determined according to the crystal manufacturer recommendations. Values of C1, C2 should be between 0pF and 4.7pF

3.3.1 Recommended 4MHz Crystal manufacturers

NDK	AT-51 GW
Epson	MA-506

The overall frequency tolerance should not exceed 200ppm.

3.4 Analog Power Pins

AVdd should be connected to Vdd. AGnd should be connected to ground. The Analog supply has to be sufficiently powered to avoid any fluctuations of power supply. It is recommended to keep the lines between 3.3V power supply and the Vdd pins as short as possible with wide PCB traces. Place a 0.1uF capacitors close to Vdd pins

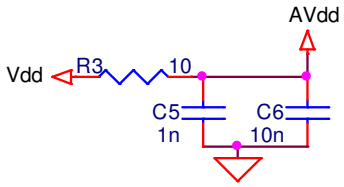

Figure 3.4 - Recommended AVdd Connection

4 OPERATION

4.1 Message Construction

The host constructs a message from bytes of data sent to its UART. The device receives this data on its HDI data-In line. The 1st low input bit (start bit) starts the signaling transmission, and the 10th high bit (stop bit) stops the transmission. If all bits, including the 10th bit, are low, the transmission continues until the HDI becomes high, but no more than 31-bit duration. It is considered as the Synch_Break Field of the LIN protocol. The stop bit stops the transmission unless a new byte is received from host. The total byte length does not change. The data latency between transmitter and receiver is about four bits.

4.1.1 Start bit

Two kinds of bytes are allowed:

1. Bytes beginning with a start bit, followed by 8 bits and ending with a stop bit.
2. Bytes beginning with a start bit followed by a number of zeros ranging from 9 to 30 bits and ending with a stop bit.

4.1.2 Commanding the SIG60

Writing and reading to/from the internal Control registers (See 4.2) using write and read commands set the device behavior.
The registers are set by power-up Reset to operate at 19.2KBps, F0 = 5.5Mhz and F1 = 6.5Mhz. Writing into the registers allows changing the selectable frequencies, the bit rate and the operating frequency. It also allows activating the automatic sleep feature and the automatic response to received bytes feature.

4.1.3 Transmit

Upon detection of a start bit in HDI, the SIG60 starts to transmit modulated signal to the Power line according to the set-up channel frequency and bit rate.
Note: *After transmission, it takes the duration of 2 bits before the device starts to listen to the Powerline.*

4.1.4 Receive

When not transmitting, the SIG60 listens to the Power line in order to:

- Detect and decode a legal signaling pattern according to the setup channel and bit rate.
- In Sleep mode, the device detects wakeup messages.
- Detects Interference signals.

Note: *After transmission, it takes the duration of 2 bits before the device starts to listen to the Powerline.*

4.2 Control Registers

4.2.1 Device operating parameters and statuses

The two internal control registers contain the device parameters and statuses:

Table 4.1 - Device Control Registers

Control Register 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	1	0	0	1
Interference detected	nLoop back	nAuto WUM	nAuto Sleep	Long WUM	Interference hopping En.	Remote Loopback	F1nF0

*Bit 0 - **F1nF0** - configure the SIG60 to operate at F0 ("0") or F1 ("1").*
*Bit 1 - **Remote Loopback** – When "1" the SIG60 will transmit back the last received byte.*
*Bit 2 - **Interference hoping** – When "1" the SIG60 will switch to the second frequency upon detecting interference on the line.*
*Bit 3 - **Long WUM** – Determines the length of the Wake Up Message (WUM) that is transmitted when the SIG60 exits the Sleep mode (initiated by its host). "1" - ~150mSec, "0" - ~75mS.*
*Bit 4 - **nAutoSleep** - "0" puts the SIG60 into Sleep mode after 8 seconds of inactivity.*

*Bit 5 - **nAuto WUM** - "1" disables the SIG60 from sending a Wake Up Message when wakened by its host.*
*Bit 6- **nLoopBack** – "1" disables loopback of HDI to HDO.*
*Bit 7 - **Interference** – "1" when interference signal is detected on the AC/DC-BUS (Read Only).*

Control Register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	1	1	1	1
Reserved	Reserved	Bit Rate (table 4.3)		Frequency select (table 4.2)			

*Bit 0-3 – **Frequencies** - Selecting pair of operating frequencies see table 4.3.*
*Bit 4-5 – **Bit rate** - Selecting operating bit rate.*

4.3 SIG60 Configuration

The SIG60 operates at default with the following parameters:
Bit rate: 19.2 kbps, F0=5.5MHz, F1=6.5MHz
The following configuration bits set the operating frequencies according to table 4.2.

Table 4.2 – F0, F1 select

Control_register1 (3:0)	F0	F1
0000	1.75Mhz	4.5Mhz
0001	1.75Mhz	5.5Mhz
0010	1.75Mhz	6Mhz
0011	1.75Mhz	6.5Mhz
0100	4.5Mhz	5.5Mhz
0101	4.5Mhz	6.0Mhz
0110	4.5Mhz	6.5Mhz
0111	4.5Mhz	10.5Mhz
1000	10.5Mhz	13.0Mhz
1001	5.5Mhz	10.5Mhz
1010	5.5Mhz	13.0Mhz
1011	6.0Mhz	10.5Mhz
1100	6.0Mhz	13.0Mhz
1101	6.5Mhz	10.5Mhz
1110	6.5Mhz	13.0Mhz
1111	5.5Mhz	6.5Mhz

Table 4.3 – bit rates selection

Bit Rates				
Control_register1 (5:4)	00	01	10	11
1.75 MHz	-	-	9.6K	19.2K
4.50 MHz	38.4K	57.6K	9.6K	19.2K
5.50 MHz	38.4K	57.6K	9.6K	19.2K
6.00 MHz	38.4K	57.6K	9.6K	19.2K
6.50 MHz	38.4K	57.6K	9.6K	19.2K
10.50 MHz	38.4K	57.6K	115.2	19.2K
13.00 MHz	38.4K	57.6K	115.2	19.2K

4.3.1 Command Mode

When in command mode, the host can configure the device according to the desired operating parameters. The device enters command mode when pin HDC is lowered to "0". When in command mode, data on the HDI pin is not transmitted to the bus, but is used to configure the SIG60. The command can be written in any of the allowed Bit Rates.
In order to write to a control register, the host sends two bytes. The first byte begins with the address of the register followed by 5(hex). The second byte is the configuration data, as shown in figure 4.1. The bytes should be sent more than 200nSec after lowering HDC.

Table 4.4 - Write Command

	Higher nibble [7:4]	Lower nibble [3:0]
First Byte	Register Address	5(hex)
Second Byte	Configuration Data	Configuration Data

Figure 4.3 shows the pins involved in the writing process:

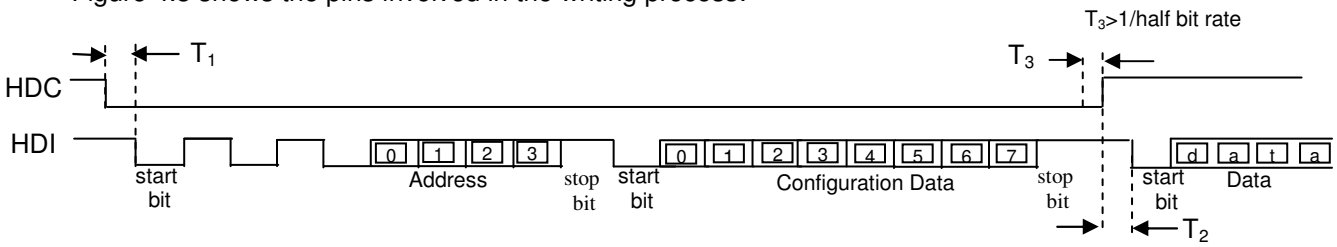

Figure 4.1 - Writing to a Control Register

In order to read from a control register, the host sends one byte. The byte should be sent more than 200nSec after lowering HDC. The byte begins with the address of the register followed by ”D”H. The SIG60 will then output the content of the register to pin HDO.

Read Command	Register Address[3:0]	D(hex)

Read Command

Figure 4.2 shows the pins involved in the reading process:

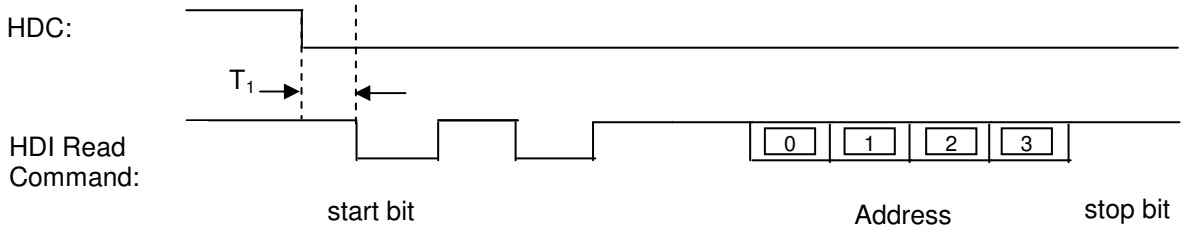

Figure 4.2 - Reading from a Control register

4.4 Loopback

The device operates like a transceiver, therefore while transmitting or writing a command the HDI signal is looped back to the HDO pin. This feature can be controlled using Bit 6 in control register 0.

4.5 Reset and Power-up

The device has internal Power-up reset. It takes 6mS until a stable operation is achieved from power-up, or from raising the nReset signal to high.

4.6 Sleep Mode

The device has three operation modes: Normal mode (normal transmitting and receiving), Sleep mode (power saving mode), and Standby mode (after waking up, while pin nSleep is low). Transitions between the modes are done via dedicated pins, or remotely, due to bus activity.

4.6.1 Entering Sleep mode

Host can move the device into Sleep mode from Normal mode either by a lowering to "0" (falling edge) pin nSleep or enabling the AutoSleep option (Setting Register 0 bit 4 to “0”). The device enters to Sleep mode and lowers output pin INH.
When AutoSleep option is enabled the device will enter Sleep mode if there was no bus activity for a period of 8 Sec. There are three ways to wakeup the device from Sleep mode.

4.6.2 Wakeup from pin nSleep

In this case, the host raises the nSleep pin. The device then enters Normal mode and raises pin INH. The device automatically transmits a wakeup message to wakeup all other devices on the bus. While transmitting this wakeup message to the bus, the device lowers pin HDO. After the transmission is complete the device raises pin HDO (can be used to signal/interrupt the host). After the transmission is completed and pin nSleep is high, the device enters Normal mode. See Figure 4.3 for signals description.

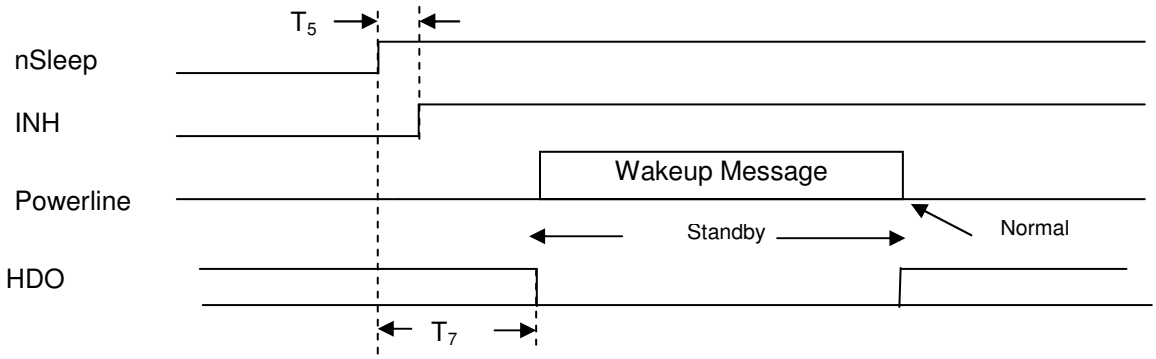

Figure 4.3 - Wakeup from nSleep

4.6.3 Wakeup from pin Wake

In this case, a transition on pin Wake (caused by an external switch of the application) is used to wake the device. The device then enters Standby mode, raises pin INH, and transmits a wakeup message to the bus. While transmitting the wakeup message to the bus, the device lowers pin HDO. After the transmission is complete the device raises pin HDO (can be used to signal/interrupt the host). After the transmission is completed and pin nSleep is high, the device enters Normal mode. The host has to raise the nSleep pin (otherwise the device will remain in Standby mode).

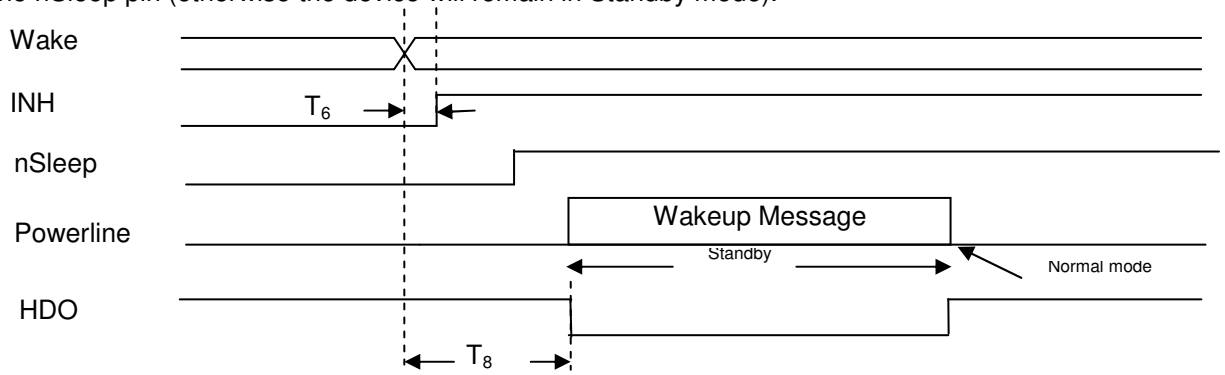

Figure 4.4 - Wakeup from Wake

4.6.4 Wakeup from bus message

During Sleep mode, the device wakes up periodically to check for activity on the bus every 32 mSec. If a wakeup message is detected, the device enters Standby mode and raises pin INH. The device then signals the host by lowering pin HDO for a minimal duration of 8 bits, and a maximal duration of about 150mSec. The host has to raise nSleep pin (otherwise the device will remain in Standby mode). After completing the reception, the device enters Normal mode. See Figure 4.5 for signals description.

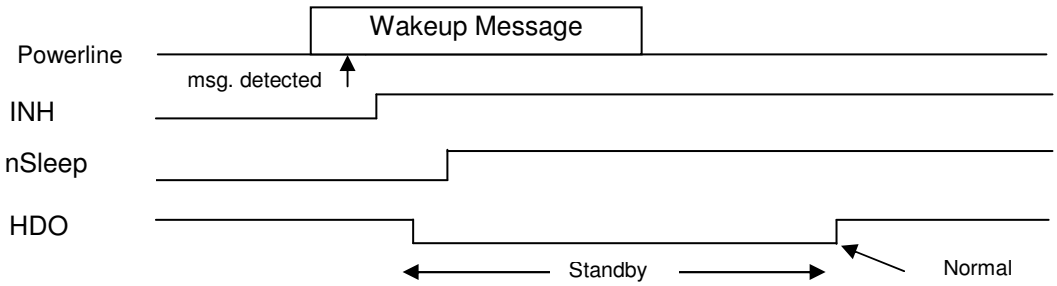

Figure 4.5 - Wakeup from bus message

4.7 Timing Characteristic

Symbol	Figure	Characteristics	Min	Max
T_1	4.3,4.4	Drop of HDC to drop of HDI	200nS	
T_2	4.3	Raise of HDC to drop of HDI	200nS	
T_3	4.3	Command stop bit to raise of HDC	Half bit rate	
T_4		Drop of nSleep to drop of INH	30uS	62uS
T_5	4.5	Raise of nSleep to raise of INH	30uS	62uS
T_6	4.6	Transact on Wake to raise of INH	30uS	62uS
T_7	4.5	Raise of nSleep to drop of HDO	92uS	124uS
T_8	4.6	Transact on Wake to drop of HDO	92uS	124uS
		Power Up or Reset to Normal mode		6mS

5 ELECTRICAL PARAMETERS

5.1 Absolute Maximal Rating

Ambient Temperature under bias	-40°C to 125°C
Storage Temperature	-55°C to 150°C
Input Voltage	-0.6V to Vdd+0.3V
Vdd Supply voltage	-0.3V to 4V

5.2 Electrical Operating Conditions

Symbol	Characteristics	Min	Typ	Max	Units	Conditions
Vdd	Supply Voltage	3.0	3.3	3.6	V	
Idd	Supply Current		40		mA	5.5MHz
Idd	Supply Current during Tx		50		mA	5.5MHz
Ipd	Power in Sleep mode		80		uA	

5.3 DC Electrical Characteristics

Symbol	Characteristics	Vdd	Typ	Units	Conditions
V_{IH}	Minimum high level input voltage	3.0	2.1	V	
V_{IL}	Maximum low level input voltage	3.0	0.9	V	
V_{OH}	Minimum high level output voltage	3.0	2.4	V	
V_{OL}	Minimum low level output voltage	3.0	0.4	V	
Iout	Maximal output current				See pin-out table
I_{IN}	Maximum input current	3.3	+/- 10	uA	

5.4 Operating Temperature

Commercial: 0°C to 70°C

Industrial: -40°C to 85°C

5.5 Mechanical Information

Package type - 28 lead QFN
See figure 5.1

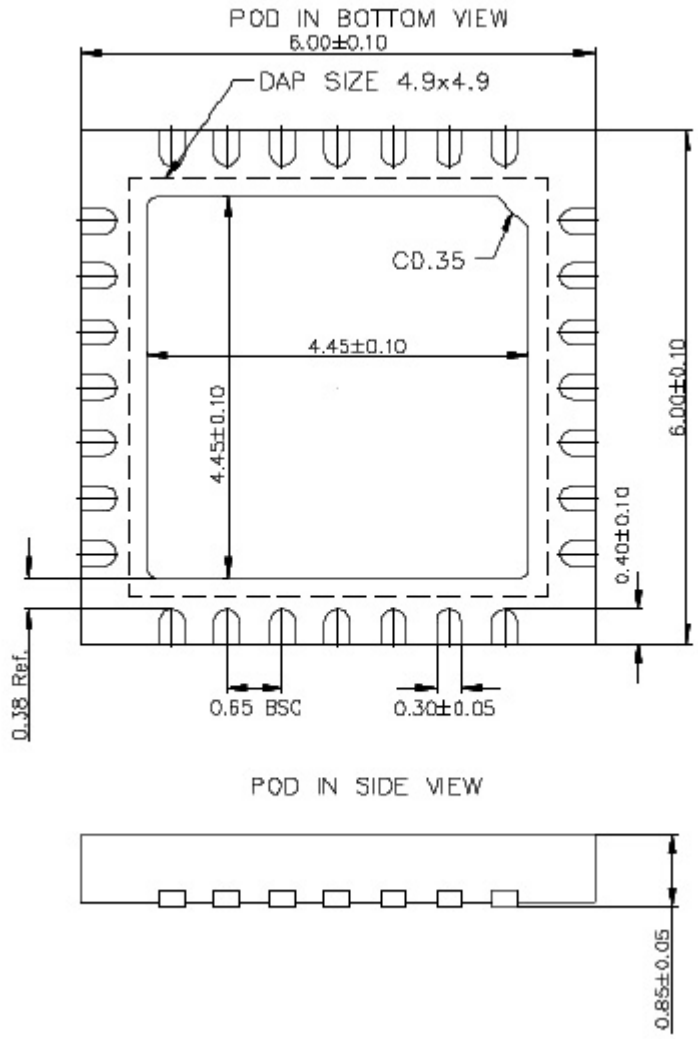

Figure 5.1 – QFN28 mechanical dimensions